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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,674	12/29/2000	Paolo Faraboschi	00-BN-059 (STMI01-00059)	9124

30425 7590 09/16/2004

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,674	FARABOSCHI ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 and new claims 21-22 have been considered. Claims 1-5, 7, 10-14, 16, and 19 have been amended as per Applicant's request. New claims 21-22 have been added.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The current abstract is merely a repeat of the independent claims. It does not describe the disclosure sufficiently nor assist readers.

5. The disclosure is objected to because of the following informalities:

a. Please revise the Summary of Invention. The current Summary of Invention is merely a repeat of the claims. This does not "set out the exact nature, operation, and purpose" nor provide "material assistance in aiding ready understanding of the patent in future searches of the invention" as set forth in MPEP § 608.01(d).

6. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1, 5, 10, 14, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what the letters "C", "N", "S", and "L" represent, i.e. whole numbers, real numbers, integers, fractions, etc.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 8-12, are 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi, U.S. Patent Number 6,167,503 (herein referred to as Jouppi) in view of Vassiliadis et al., U.S. Patent Number 5,051,940 (herein referred to as Vassiliadis).

11. Referring to claims 1, 10, 21, and 22, Jouppi has taught a processing system comprising:

a. A data processor (Applicant's claim 10) (Jouppi column 2, lines 61-64 and Figure 1);

b. A memory coupled to said data process (Applicant's claim 10) (Jouppi column 3, liens 16-25 and Figure 1);

c. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Applicant's claim 10) (Jouppi column 3, lines 16-65 and Figure 1);

d. Wherein said data processor comprises:

i. C execution clusters (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters capable of executing instruction bundles comprising from one to S syllables (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B);

ii. An instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising C*L syllables (Applicant's claims 1 and 10) (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

iii. An instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

iv. Alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles (Applicant's claims 1 and 10) (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

12. Jouppi has not taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10).

d. Aligning said syllables with correct ones of said lanes (Applicant's claims 21 and 22).

13. Vassiliadis has taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40).

d. Aligning said syllables with correct ones of said lanes (Applicant's claims 21 and 22) (Vassiliadis column 2, lines 40-57). In regards to Vassiliadis, the only way for the instruction pairs to be issued simultaneously is for them to be associated with the correct lanes.

14. A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

15. Referring to claims 2 and 11, Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

16. Referring to claims 3 and 12, Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles (Jouppi column 4, lines 53-63; Figure 2A; and Figure 2B).

17. Referring to claims 8 and 17, Jouppi has not taught wherein L=4. Vassiliadis has taught a pipeline with N-stages, which includes 4 stages. In regards to Vassiliadis, it does not matter how many stages the pipeline is. That is the length of a pipeline, i.e. the number of stages, is dependent on how much potential improvement a designer desires (Vassiliadis column 1, lines 12-40). A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been

obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

18. Referring to claims 9 and 18, Jouppi has taught wherein C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42).

19. Referring to claim 19, Jouppi has taught for use in a data processor C execution clusters (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters capable of executing instruction bundles comprising from one to S syllables (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), a method of routing instruction bundles into the L lanes in the C execution clusters comprising the steps of:

a. Fetching cache lines from an instruction cache, each of said cache lines comprising C*L syllables (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

b. Issuing complete instruction bundles toward the C execution clusters (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

c. Routing each of the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one of (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B):

i. At least one address bit associated with each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

ii. At least one address bit associated with at least one syllable in each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

iii. A cluster bit associated with each of the complete instruction bundles (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

20. Jouppi has not taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10).

21. Vassiliadis has taught

a. An instruction execution pipeline having N processing stages (Vassiliadis column 1, lines 7-40);

b. Wherein each of said instruction execution pipelines is L lanes wide (Vassiliadis column 1, lines 7-40); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Vassiliadis column 1, lines 7-40).

22. A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

23. Referring to claim 20, Jouppi has taught wherein C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42). Jouppi has not taught wherein L=4. Vassiliadis has taught a pipeline with N-stages. In regards to Vassiliadis, it does not matter how many stages the pipeline is. That is the length of a pipeline, i.e. the number of stages, is dependent on how much potential improvement a designer desires (Vassiliadis column 1, lines 12-40). A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

24. Claims 4-7 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi in view of Vassiliadis as applied to claims 1 and 10 above, and further in view of Sachs et al., U.S. Patent Number 5,560,028 (herein referred to as Sachs). Jouppi has taught wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

a. Said at least one address bit associated with each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4,

lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

b. At least one address bit associated with at least one syllable in each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

c. A cluster bit associated with each of said complete instruction bundles (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

25. Jouppi has not taught

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundle (Applicant's claims 4 and 13);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundle to any one of said C execution clusters (Applicant's claims 5 and 14); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claims 6 and 15).

26. However, Jouppi has taught instruction dispersal circuitry (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B). Sachs has taught instruction dispersal circuitry

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles (Applicant's claim 4) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said C execution clusters (Applicant's claim 5) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claim 6) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10).

27. A person of ordinary skill in the art at the time the invention was made would have recognized that the instruction dispersal circuitry ensures the correct execution cluster executes the instruction bundles, thereby ensuring valid and correct data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dispersal circuitry of Sachs in the device of Jouppi to ensure valid and correct data.

Response to Arguments

28. Examiner withdraws the objections to the drawings in favor of amendments to the Specification and remarks found on page 16 of Applicant's response.

29. Examiner withdraws the objection to the specification regarding updating the information regarding related U.S. Patent Applications in favor of amendments to the Specification.

30. Examiner withdraws the objection to the claims in favor of amendments to the claims and remarks found on page 17 of Applicant's response.

31. Examiner withdraws 35 U.S.C. §112 Rejection regarding claim 19 being indefinite.

32. Examiner maintains the objection to the specification regarding the abstract. As stated in the previous action, "The form and legal phraseology often used in patent claims, such as 'means' and 'said,' should be avoided." The language in the abstract follows very closely to the claims and does not sufficiently describe the disclosure. The claims of an invention do not necessarily "sufficiently describe" the disclosure. The language is also contains legal phrases and terms from the claims.

33. Examiner maintains the objection to the specification regarding the Summary of the Invention. The Summary of the Invention is required to "be commensurate with the invention as claimed." However, this does not mean the claims should be copied into the Summary of the Invention. The Summary of the Invention should "set out the exact nature, operation, and purpose" while providing "material assistance in aiding ready understanding of the patent in future searches of the invention." Even though limitations are not read from the specification, the claims are read in light of the specification. When the claims are merely copied and pasted into sections of the specification there is no "material assistance in aiding understanding of the

patent in future searches of the invention." Should there be no explanation of the "exact nature, operation, and purpose" of the invention in the specification other than language found in the claims, the claims may be interpreted however convenient during future searches, even when the claim language should not be applicable due to the nature of the invention.

34. Examiner maintains the 35 U.S.C. §112 Rejection regarding claims 1, 5, 10, and 14 as being indefinite. The letters "C", "N", "S", and "L" are unclear as to what type of number, i.e. whole numbers, integers, fractions, etc., is being referred to in the claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

35. Applicant's arguments filed 21 June 2004 have been fully considered but they are not persuasive.

36. Applicant argues on in essence pages 19-21

> Applicant respectifully submits that such a feature is not found in either of the cited references nor can such a feature be found in a combination of the cited references.
>
> The cited passages in *Vassiliadis* recite an instruction execution pipeline that has N processing stages. However, the cited passages of *Vassiliadis* do not teach or suggest that the instruction execution pipeline is "L lanes wide."

37. This has not been found persuasive. Vassiliadis teaches pipelining and executing instructions in parallel, i.e. a superscalar machine (Vassiliadis column 2, lines 35-55). In order to execute instructions in parallel in a superscalar machine, lanes are needed to correctly simultaneously issue multiple instructions at once. Vassiliadis states "...a 'superscalar machine'

in which a number of instructions are grouped strictly...for simultaneous issue. Assuming hard is designed to support the simultaneous issue of two instructions, a compound instruction machine would pair (Vassiliadis column 2, lines 43-47)..." This means that there is hardware in the system which allows multiple instructions to issue at once, therefore the lanes to issue the instructions must exist for simultaneous issue to occur, especially if the correct simultaneous issue is to occur. Should the issue lanes not exist, the instructions would only be issued sequentially and issuing the instruction pairs in Vassiliadis on column 2, lines 54-56 would not be possible. The instruction lanes are inherent in order for the instruction pairs to be issued simultaneously.

Conclusion

38. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

39. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

41. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

42. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
September 14, 2004

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